

## **ABSTRACT OF THE DISCLOSURE**

The present invention relates to a method for manufacturing a semiconductor device, and more particularly, to a method for manufacturing a semiconductor device, in which a LDD region is formed by implanting phosphor or as  
5 impurities, then a high concentration As is implanted to a bit line contact region and a gate poly and then phosphor is implanted again to the bit line contact region and the gate poly, so that the high concentration As can be surrounded by the phosphor implanted two times, whereby the resistance of the bit line contact and a data path can be maintained low and the leakage current and junction capacitance caused by the  
10 high implanting concentration of As of the bit line contact junction can be drastically lowered, thus improving the characteristics of a DRAM, and whereby the space between a MOS capacitor and a gate is reduced to minimize the generation of the Tr-off current and the capacitor region can be increased to increase the capacitance of the device.